Code No: P21ITT02

HALL TICKET NUMBER

PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE

(AUTONOMOUS)

II B.TECH I SEMESTER END REGULAR EXAMINATIONS, JAN - 2023

COMPUTER ORGANIZATION

(Common to IT,CSE(IOTCSBT), AIDS,AIML Branches)

Time: 3 hours Max. Marks: 70

Answer all the questions from each UNIT (5X14=70M)

Q.No.		Questions	Marks	CO	KL
		UNIT-I			
1.	a)	Explain operations on unsigned binary numbers and Perform the subtraction with the following unsigned binary numbers using 2's compliment. i) 11010-10000 iii) 11010-1101 ii) 100-110000 iv) 1010100-1010100	[7M]	1	2
	b)	Write and explain different types of computers based on the functions they perform.	[7M]	1	3
		OR			
2.	a)	Explain the fixed point representation with an example.	[7M]	1	3
	b)	Explain about the error detection codes.	[7M]	1	2
		UNIT-II			
3.	a)	Show to construction of bus system with four registers and explain various functions used to select registers by bus.	[7M]	2	4
	b)	Explain the various arithmetic micro operations.	[7M]	2	3
		OR			
4.	a)	Describe the memory reference instructions with an example.	[7M]	2	4
	b)	Explain the input output configuration with interrupts. And explain the flowchart for interrupt cycle with an example.	[7M]	2	2
		UNIT-III			
5.	a)	Explain about the RISC architecture.	[7M]	3	3
	b)	Explain various instruction formats based on the number of address fields used in the instruction format with an example.	[7M]	3	2
		OR			
6.	a)	Differentiate between hardwired and micro programmed computers.	[7M]	3	4
	b)	Explain the selection of address for control memory.	[7M]	3	5
		UNIT-IV			
7.	a)	Explain about the auxiliary memory.	[7M]	4	3
	b)	Explain the relation between address and memory space in a virtual memory systems.	[7M]	4	3
		OR			
8.	a)	Explain about different types of memory mapping techniques?	[7M]	4	3
	b)	Explain the READ and WRITE operations in Associative Memory.	[7M]	4	3
		UNIT-V			
9.	a)	Describe the Flynn's Classification of computers with Parallel Processing?	[7M]	5	4
	b)	Differentiate serial arbitration logic and parallel arbitration logic with neat sketches.	[7M]	5	5
		OR			
10.	a)	Explain Array Processing with neat diagram?	[7M]	5	3
	b)	Describe RISC Pipelining System?	[7M]	5	3

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